

WHAT IS CLAIMED IS:

1. A digital processing system comprising:
a first semiconductor device having a plurality of computation nodes;
a second semiconductor device having a microprocessor-based node adapted to function as a system controller and a plurality of computation nodes; and
a bus for inter-connecting said first semiconductor device to said second semiconductor device in a ring topology whereby the microprocessor-based node allocates a plurality of operations among said computation nodes of said first and second semiconductor devices over said inter-connecting bus and receives the results of said operations over said inter-connecting bus.
2. The digital processing system of claim 1 wherein said computation nodes on said first and second semiconductor devices include at least one of the following node types: an arithmetic node, a bit manipulation node, a reduced instruction set processing node and a finite state machine node.
3. The digital processing system of claim 1 wherein the digital system includes a plurality of nodes each of which can perform at least one type of operation and wherein said microprocessor node allocates functions temporally and spatially among the nodes of said first and second semiconductor devices.
4. The digital processing system of claim 1 further comprising:
a remote processor; and

a second bus for interfacing said first and second semiconductor device to said remote processor.

5. The digital processing system of claim 4 further comprising:
a real-time data source; and
a third bus for interfacing said first and second semiconductor device to said real-time data generator.

6. The inter-connecting bus of the digital processing system of claim 1 further comprising:
a plurality of logic elements, each closely proximate to a corresponding output pad of said first semiconductor device, for sending data and control signals;
a plurality of logic elements, each closely proximate to a corresponding input pad of said second semiconductor device, for receiving said data and control signals;
and
means for synchronously transferring data and control logic by clocking the logic elements of said first and second semiconductor devices.

7. The digital processing system of claim 6 further comprising:
a first core logic clock signal provided to each of said nodes of said first semiconductor device;
a second core logic clock signal provided to each of said nodes of said second semiconductor device, said first and second core logic clocks having substantially the same frequency and phase;

a first bus clock for clocking said logic elements of said first semiconductor device at a selected rate where said first bus clock is derived from said first core logic clock;

a second bus clock for clocking said logic elements of said second semiconductor device at said selected rate where said second bus clock is derived from said second core logic clock; and

a synchronizing signal generated by said first semiconductor device.

8. The digital processing system of claim 1 further comprising:

a first core logic clock signal provided to each of said nodes of said first semiconductor device;

a second core logic clock signal provided to each of said nodes of said second semiconductor device, said first and second core logic clocks having substantially the same frequency and phase; and

means for synchronizing the transfer for data and control signals from said first semiconductor device to said second semiconductor device, said synchronizing means derived from said first core logic clock signal.

9. The synchronizing means of claim 8 further comprising:

a first bus clock for clocking said logic elements of said first semiconductor device at a selected rate where said first bus clock is derived from said first core logic clock;

a second bus clock for clocking said logic elements of said second semiconductor device at said selected rate where said second bus clock is derived from said second core logic clock; and

a signal, generated by said first semiconductor device, for indicating valid data and control signals to said second semiconductor device.

10. The digital processing system of claim 1 wherein said first and second semiconductor devices are coupled in a ring with said inter-connecting bus coupling an output port of said first semiconductor device to an input port of said second semiconductor device and further coupling an output port of said second semiconductor device to an input port of said first semiconductor device.

11. The digital processing system of claim 1 wherein said microprocessor-based node determines whether a packet received on said second bus is addressed to a node on either said first or second semiconductor device.

12. The digital processing system of claim 11 wherein said microprocessor-based node passes said packet to one of said plurality of computation nodes on said first semiconductor device if said packet is addressed to a node on said first semiconductor device or transferring said packet to one of said plurality of computation nodes on said second semiconductor device if said packet is addressed to a node on said second semiconductor device where said packet is transferred on said inter-connecting bus.

13. The digital processing system of claim 11 wherein said packet includes a device identification field.

14. A digital processing system comprising a plurality of adaptive computing engines each having a plurality of computation nodes; said adaptive computing engines coupled in a ring topology by a bus, said bus adapted for passing packets between said computation nodes; one of said adaptive computing engines having a kernel node, said kernel node adapted for determining whether a packet is intended for one of said computation nodes and for discarding packets intended for computational nodes that are not part of said digital processing system.

15. The digital processing system of claim 14, wherein each of said adaptive computing engines includes a device identification number and said packet includes a device identification field.

16. The digital processing system of claim 15, wherein each adaptive computing engine includes an output port coupled to an input port of the next adjacent adaptive computing engine in said ring.

17. The digital processing system of claim 16, wherein said ring comprises two, three or four adaptive computing engines.

18. The digital processing system of claim 14 wherein said output port comprises a plurality of D type flip flops coupled to a corresponding plurality of D type flip flops at said input port.

19. A method for transferring information from one adaptive computing engine having a plurality of computational nodes to another adaptive computing

engine having a second plurality of computational nodes, said method comprising the steps of:

Generating a common clock signal routed to at least two adaptive computing engines;

Requesting to transfer information from one adaptive computing engine to another adaptive computing engine;

Offering to receive said information;

Transferring said information from a D type flip flop associated with said output port to a D type flip flop associated with said input port;

Controlling the transfer of said information from said D type flip flop associated with said output port with a first clock derived from said common clock signal;

Controlling the receipt of said information by said D type flip flop associated with said input port with a second clock derived from said common clock signal; and

Generating a signal to define a window during which the transfer of said information is valid.

20. The method of claim 19 further comprising the step of coupling up to four adaptive computing engines in a ring topology.

21. The method of claim 20 further comprising the steps of:

designating one of said adaptive computing engines in said ring to function as a kernel node;

initially receiving said information at said designated adaptive computing engine; and

determining whether said information is intended for one of the adaptive computing engines in said ring.

22. The method of claim 21 further comprising the step of transferring said information from adaptive computing engine to adaptive computing engine around said ring until said information arrives at the intended adaptive computing engine.

23. The method of claim 22 further comprising the step of discarding said information if said kernel node determines the information is not intended for one of the adaptive computing engines in said ring.

24. The method of claim 23 further comprising the step of passing said information from adaptive computing engine to adaptive computing engine around said ring until said information arrives at its intended destination adaptive computing engine.

25. The method of claim 21 further comprising the step of providing a FIFO buffer, coupled to said D type flip flop associated with said output port, for retaining information until the input port offers to receive information.

26. The method of claim 25 further comprising the step of providing a FIFO buffer, coupled to said D type flip flop associated with said input port, for receiving information after closing said window that indicates the transfer of said information is valid.

27. A digital device comprising:
a processor;
a user interface controlled by said processor;
memory associated with said processor; and
a plurality of adaptive computing engine devices each having a plurality of computation nodes; said adaptive computing engine devices coupled in a ring topology by a first bus; at least one of said adaptive computing devices coupled to said processor and said memory by a second bus so that each of said plurality of computation nodes can access said memory..

28. The digital device of claim 27, further comprising:
a real-time data source; and
a third bus coupling said real-time data source to at least one of said plurality of adaptive computing engine devices.

29. The digital device of claim 27, wherein each of said plurality of adaptive computing engine devices is coupled to said second bus.

30. The digital device of claim 27, wherein said first bus couples an output port of each device to an input port of a next device in said ring.

31. The digital device of claim 27, wherein said first bus includes:
a plurality of D type flip flops, each closely proximate to a corresponding output pad of output port, for sending data and control signals;

a plurality of D type flip flops, each closely proximate to a corresponding input pad of said output port, for receiving said data and control signals; and
means for synchronously transferring data and control logic by clocking the logic elements of said first and second semiconductor devices.

32. The digital device of claim 27, wherein one of said plurality of adaptive computing engine devices includes a kernel node.

33. An integrated circuit comprising:
a plurality of computational elements including a plurality of arithmetic nodes, a plurality of bit-manipulation nodes, a plurality of finite state machine nodes, and a plurality of input/output nodes;
a first and a second processing node each having a core processor based on a common architecture;
a first memory associated with said first processing node;
a second memory associated with said second processing node;
a first node wrapper for coupling said core processor of said first processing node to said first memory and to said computational elements;
a second node wrapper for coupling said core processor of said second processing node to said second memory and to said computational elements; and
means for interconnecting said computational elements and said first and second processing nodes to define a selected task to achieve a desired functionality.

34. The integrated circuit of claim 33 further comprising means for temporally adapting said second node and said computational elements to perform a selected function.

35. The integrated circuit of claim 34 wherein said temporal means further comprises executable code defining said selected function stored in at least said first memory.

36. The integrated circuit of claim 35 wherein said executable code is downloaded from the Internet by said first processing node.

37. The integrated circuit of claim 36 wherein said executable code comprises operating system code.

38. The integrated circuit of claim 37 wherein said first processing node initiates the temporal adaptation of said computational elements and said second processing node to perform said selected function.

39. The integrated circuit of claim 33 wherein said computational elements include a plurality of arithmetic nodes, a plurality of bit-manipulation nodes and a plurality of finite state machine nodes.

40. The integrated circuit of claim 33 further comprises a plurality of said second processing nodes each of which is coupled to said first processing node and computational elements by said interconnecting means.

41. An adaptive computing engine comprising:

- a controller node having:
- a core processor for executing operating system code;
- a memory for storing operating system executable code;
- means for transferring operating system executable code and data from said memory to said core processor;

a plurality of computational elements adapted to perform a selected function at least one of said computational elements having:

- a RISC processor for executing code;
- a memory for storing executable code;
- means for transferring executable code and data from said memory to said RISC processor; and

a temporal interconnecting matrix coupling said controller node to said plurality of computational elements to perform a user selected function.

42. An adaptive computing engine having a plurality of computational elements and a temporal interconnecting matrix for connecting said computational elements, said adaptive computing engine comprising:

- a controller node for adapting said computational elements in response to perform a selected function, said controller node having:

- a core processor for executing operating system code;
- a memory for storing operating system executable code;
- means for transferring operating system executable code and data from said memory to said core processor;

a set of registers associated with said core processor;

a node wrapper, coupled to said core processor, for receiving an input stream from an external source, said input stream having configuration information and executable code and passing said information to said core processor; and

means for accessing said set of registers;

an interrupt controller for detecting interrupt conditions from said node wrapper and internally.

43. The adaptive computing engine of claim 42 further comprising means for accessing said core processor and said memory to debug error conditions.

44. The adaptive computing engine of claim 42 further comprising means for handling node-to-node communication.

45. The adaptive computing engine of claim 42 further comprising executable code for controlling the temporal adaptation of said computation elements in response to configuration information.

46. The adaptive computing engine of claim 45 further comprising means for controlling the initiation of operation of said computational element upon reset or power on.

47. The adaptive computing engine of claim 46 further comprising a programmable scalar node having:

a core processor for executing instructions;

an instruction memory for storing said instructions;
a data memory;
means for transferring instructions from instructions memory to said core processor and for transferring data to said core processor from said data memory;
a set of registers associated with said core processor; and
a node wrapper, coupled to said core processor, for receiving an input stream from controller node, said input stream having configuration information; means for accessing said set of registers; and an interrupt controller for detecting interrupt conditions.

48. The adaptive computing engine of claim 47 further comprising:

a data cache; and
an instruction cache.